Clock System Status Report

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G-2 Detector Meeting

Clock for DAQ

- Need a stable, uniform timebase for DAQ
  - ✓ 500 MHz Waveform digitizers, Tracker TDCs, other components
- Timing specifications:
  - ✓ Jitter << 2ns (i.e. smaller than WFD precision)
  - ✓ Systematic variation: <10 ps across single spill (~200 μs)
  - ✓ Drift over longer times: should be small
    - GPS Disciplined Oscillator insure this: needs monitoring.

Baseline design

Courtesy of Kevin Pitts

readout

time stamp

Today' topic

GPS disciplined oscillator

10 MHz

Frequency synthesizer

50.000xxx MHz

fanouts

Amplitude measure

readout

Precision freq counter

Frequency synthesizer

61.740yyy MHz

NMR DAQ

Calorimeter WFD µTCA

AMC13

x24

double-shielded coax

Tracker µTCA

AMC13

x2

other consumers

- Clock distributed as sine wave
  - Double shielded cable to minimize pickup
- Separate blinding for ω_a,ω_p
  - Same GPSDO source

Meridian

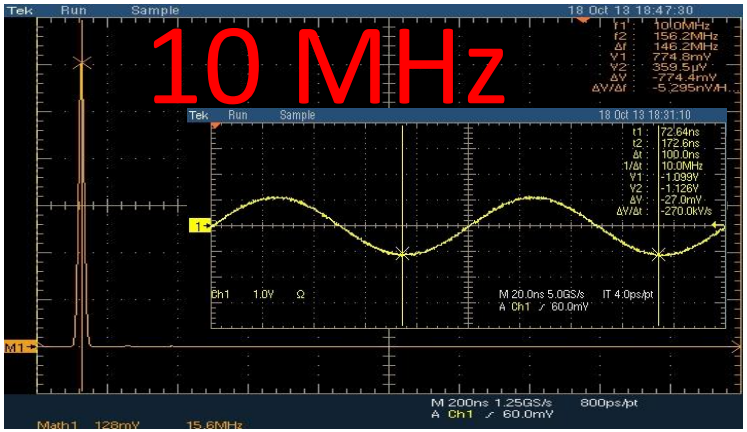
Precision GPS TimeBase

EndRun TECHNOLOGIES

"Smarter Timing Solutions"

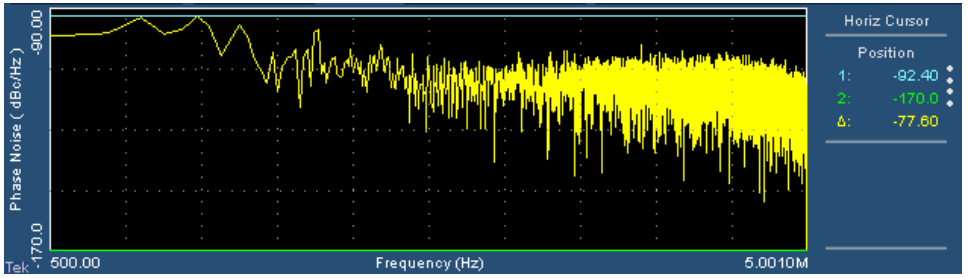
FEATURES

- Modular, plug-and-play design, accepts a variety of field-installable options.
- Timing accuracy: < 10 nanoseconds RMS to GPS.
- Frequency accuracy: $< 1 \times 10^{-13}$.
- 1 PPS output.



- **Low Phase Noise (LPN) 10 MHz Sine wave with exceptional spectral purity**

LPN<-80dBc/Hz

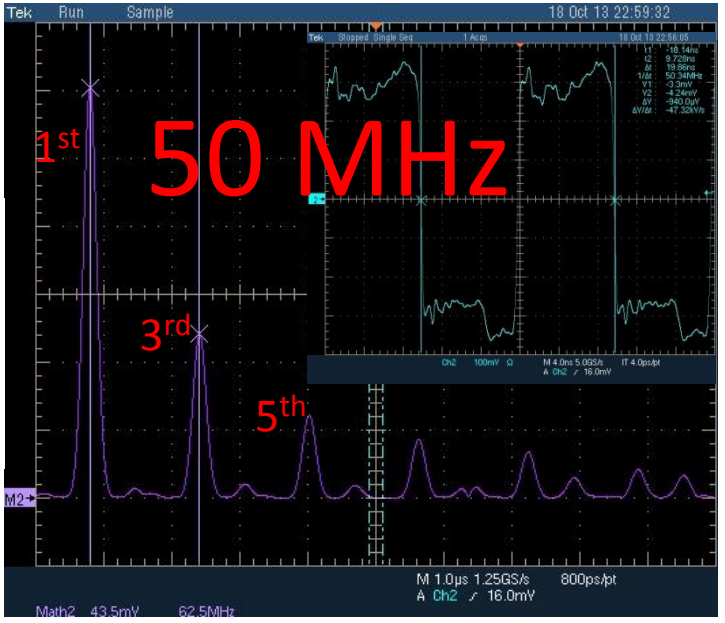


Model KY3840A Frequency Synthesizer 29 to 3840 MHz

Product Features

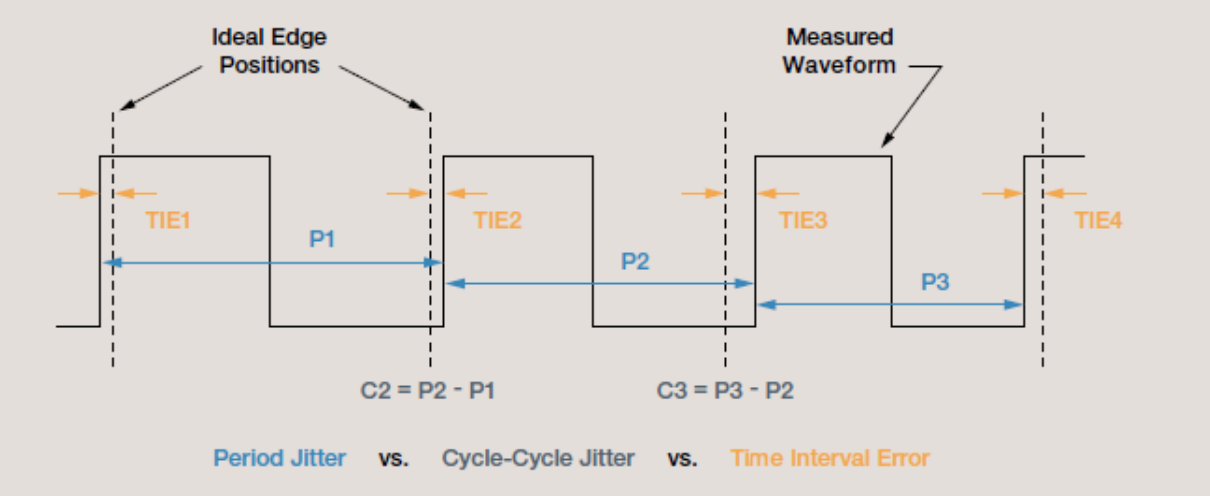
- 29 to 3840 MHz frequency range
- 1 Hz tuning resolution
- +10 dBm output power
- Single +15 Vdc supply
- Selectable RS-232 or 4-Wire serial control
- 6 millisecond tuning time
- Programmable reference trim
- ±1.0 ppm internal reference stability
- 10 MHz reference output
- Selectable frequency external reference input
- -70 dBc non-harmonic spurious
- Internal temperature monitor
- -30°C to +70°C operating temperature
- Phase noise:
  - -110 dBc/Hz, 10 kHz Offset at 1 GHz
  - -130 dBc/Hz, 10 kHz Offset at 100 MHz

(Un)Blinding



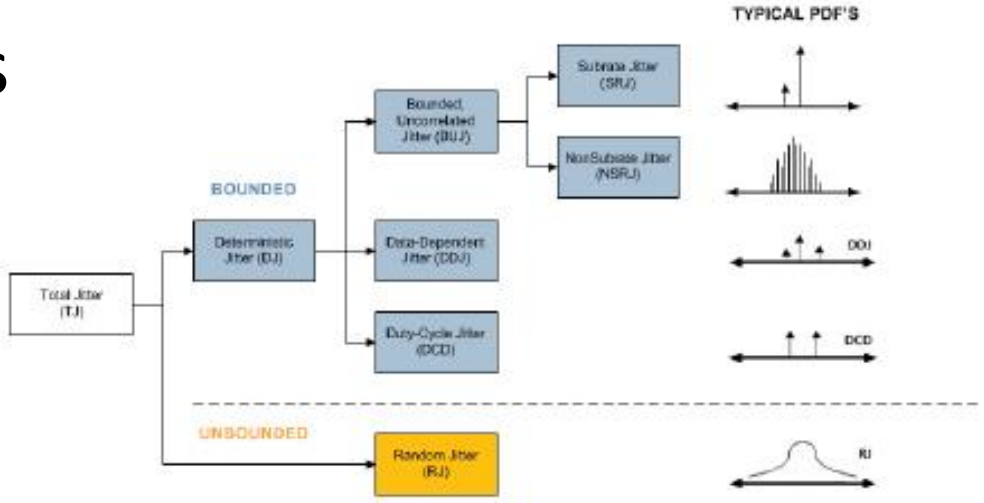
Unwelcome companion

"Jitter is defined as the short-term variations of a digital signal's significant instants from their ideal positions in time."

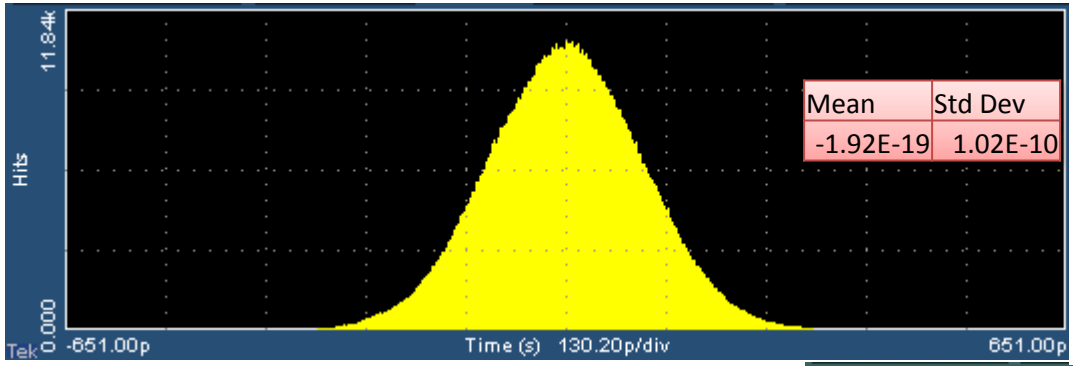


Time Jitter evaluated using TIE measurements

Used standard tools (TDSJIT3 Jitter Analysis Software, Tektronix)



TIE – Clock only

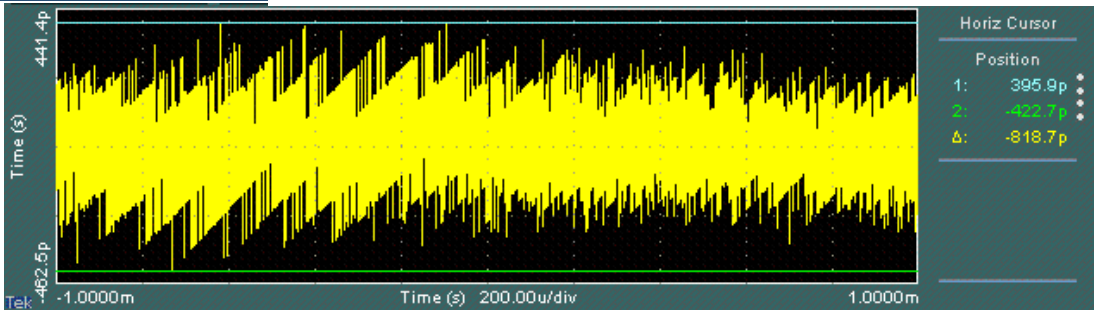


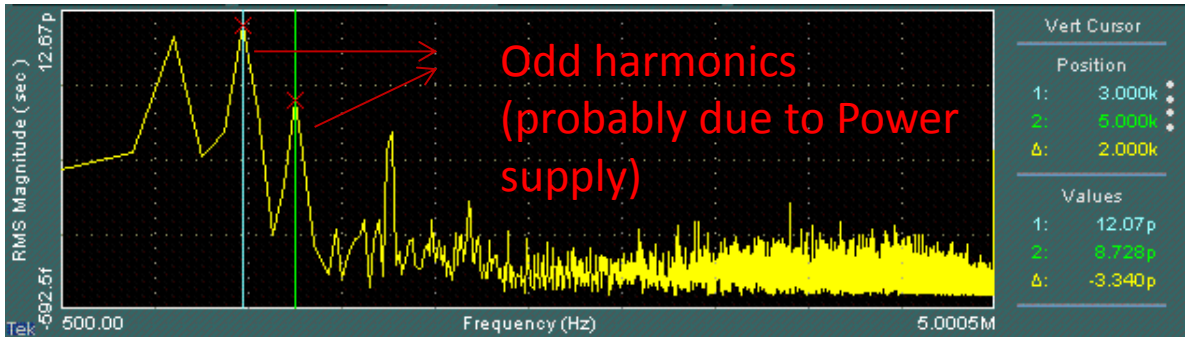
Time Jitter dominated by Random Noise

Time accuracy <1 ns

(<10 ns claimed)

Periodical modulation

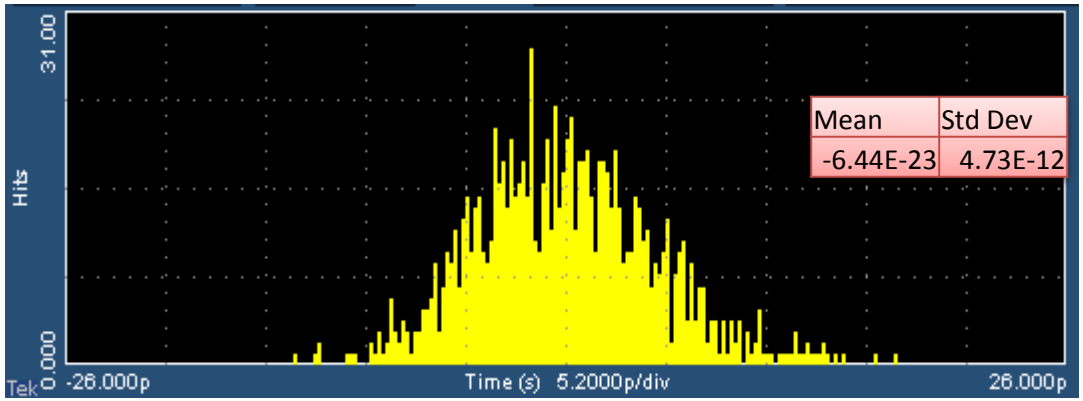




Jitter Component	Results (s)
Random(RMS)	1.02E-10
Deterministic(Pk-Pk)	2.86E-11
Periodic	2.86E-11
Duty Cycle	0
Data Dependent	0
Total@BER (Pk-Pk)	1.41E-09
Eye Opening @ BER (UI)	0.985872

O(ns) Total Jitter seems not meet our requirements.

TIE – Clock+Synt+Fanout

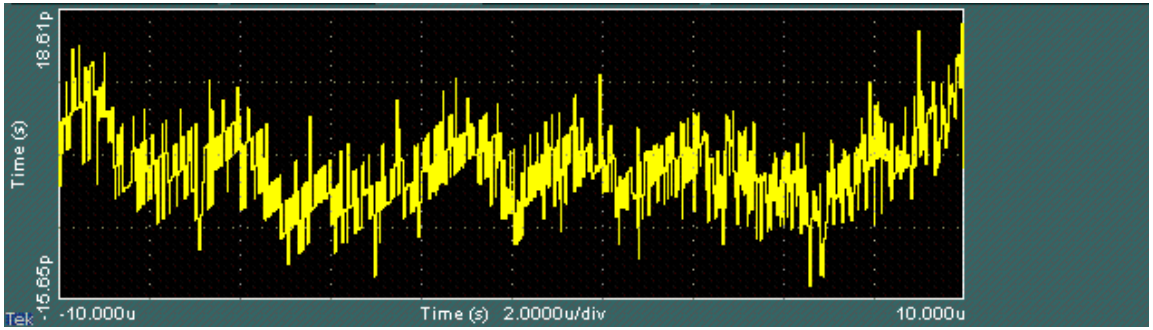


Broader distribution: Deterministic Jitter competes with Random

More clear modulation but Time accuracy < 40 ps:

Synth. PLL circuit effect

Jitter Component	Results (s)
Random(RMS)	4.73E-12
Deterministic(Pk-Pk)	8.65E-12
Periodic	8.65E-12
Duty Cycle	0
Data Dependent	0
Total@BER (Pk-Pk)	4.99E-11
Eye Opening @ BER (UI)	0.997506



~50 ps Total Jitter: <<2 ns as required but systematic variations < 10 ps not assured.

Final Clock System

- …on the way for a test clock system:
  - ✓ Provides “realistic” signals for testing
  - ✓ Preliminary values to use for simulation purpose.

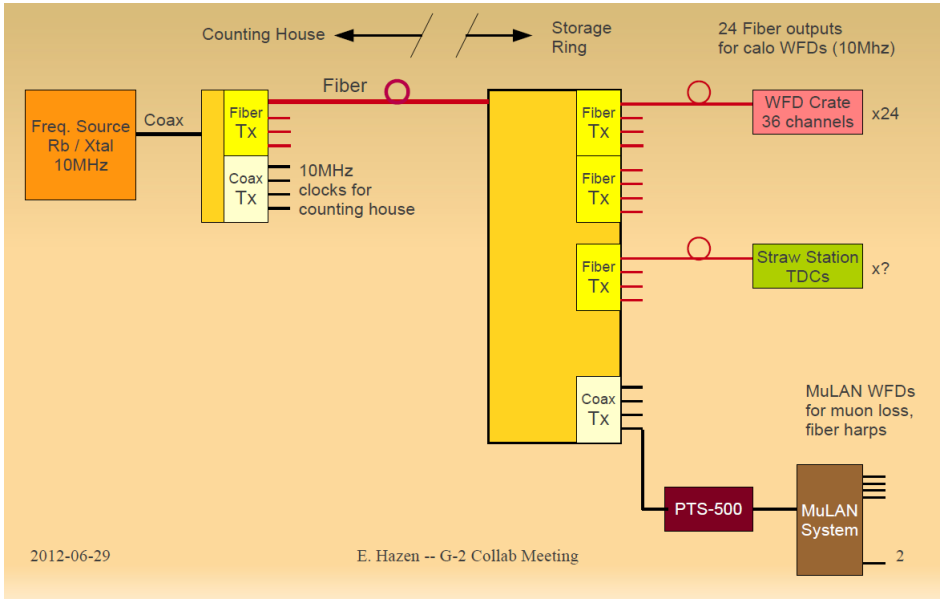
However…..

Control signals

- Clock system will also distribute control signals to front end/DAQ.
- Possible signals
  - Begin fill
  - End fill
  - Global reset/sync
- Options:
  - Parallel path (copper)
  - Encoded with clock (TTC) if optical

‘Clock’ never stops…

- Need to investigate fiber optic distribution scheme



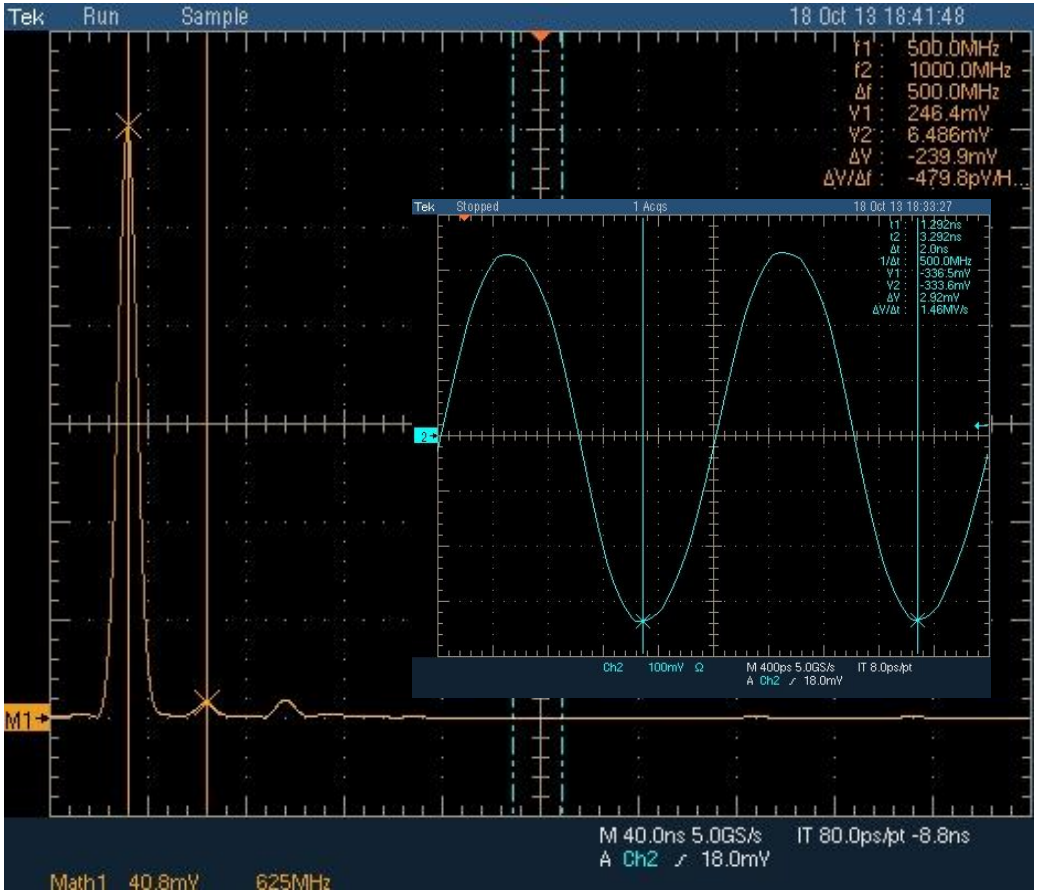
- Need to evaluate jitter impact (systematics) on final measurement.
  - ✓ Simulate calorimeter, photomultiplier and realistic waveforms
  - ✓ Include clock system tests infos in the simulation.

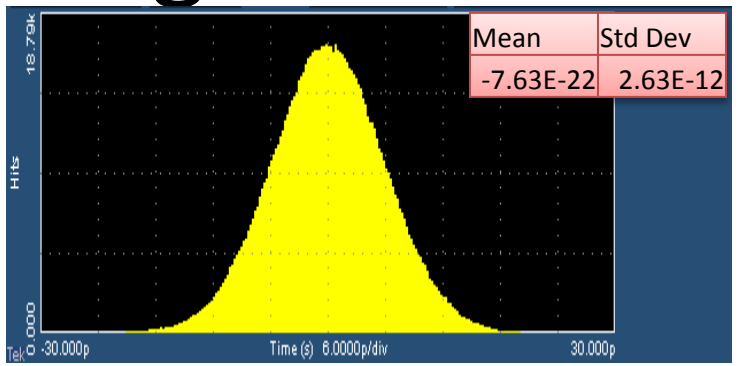
Conclusions

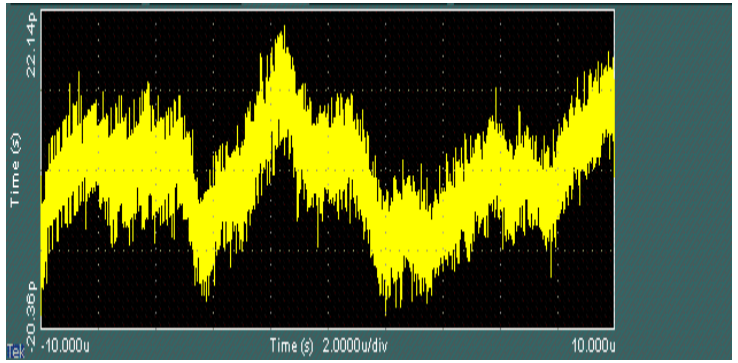
- Test prototype clock system:
  - ✓ First components under studies
  - ✓ Baseline design prototype almost realized
- Simulation effort:
  - ✓ Trying to add time-jitter informations
- New clock distribution scheme to investigate

Backup

500 MHz clock signal







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Deterministic(Pk-Pk)	1.63E-11
Periodic	1.63E-11
Duty Cycle	0
Data Dependent	0
Total@BER (Pk-Pk)	4.91E-11
Eye Opening @ BER (UI)	0.975428

~50 ps Total Jitter: <<2 ns as required but systematic variations < 10 ps not assured.